UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,133	09/10/2003	Per Hammarlund	Intel 2207/618602	4796

25693 7590 05/11/2007

KENYON & KENYON LLP
RIVERPARK TOWERS, SUITE 600
333 W. SAN CARLOS ST.
SAN JOSE, CA 95110

EXAMINER	
CHEN, TE Y	

ART UNIT	PAPER NUMBER
2161	

MAIL DATE	DELIVERY MODE
05/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/659,133
Filing Date: September 10, 2003
Appellant(s): HAMMARLUND ET AL.

Jeffrey R. Joseph
For Appellant

SUPPLEMENTAL EXAMINER'S ANSWER

This examiner's answer is supplemental because the Heading #11: Related Proceedings Appendix is missing from the previous copy mailed on March 06,2007.

This is in response to the appeal brief filed on November 17, 2006 appealing from the Office action mailed May 23, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,644,753	Ebrahim et al.	7-1997
5,867,511	Arimilli et al.	2-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-11,13, 18 and 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebrahim et al. (U.S. Patent No. 5,644,753) in view of Arimilli et al. (U.S. Patent No. 5,867,511).

As to claim 2, Ebrahim et al. (hereinafter referred as Ebrahim) discloses an apparatus [e.g., col. 1, lines 8-16; Fig(s). 1 and 12 and associated texts], comprising:

a) a resource having a plurality of elements [e.g., the units: 108, 109, 120, 134, 140, etc. Fig. 1];

b) at least first and second components access the elements of the resource [e.g., the units 102-1 to 102-n, 108, etc. Fig. 1 and associated texts]

c) an access controller [e.g., the unit 110, Fig. 1 and 5] coupled to the resource and the at least first and second components [e.g., the units 102-1 to 102-n, Fig. 1] to stored a first mask value [e.g., The UPANUM field 182, Fig. 5 and associated texts], wherein access to the elements of the resource by the first and second components is controlled based on the first mask value [e.g., col. 21, line 58 – col. 22, line 4 and col. 22, lines 8-10].

Ebrahim does not specifically disclose the elements of the resource are selectively partitioned and access the partitioned elements thereby.

However, Arimilli et al. (hereinafter referred as Arimilli) discloses the claimed features [e.g., col. 2, lines 8-58 & the Alternate Victim Selection Logic, Fig. 3 and associated texts].

Ebrahim and Arimilli are both in the same field to improving shared cache processing via memory mask, therefore, with the teachings of Ebrahim and Arimilli in

front of him/her, it would have been obvious for an ordinary skilled person in the art at the time the invention was made being motivated to combine the well-known technique as taught by Arimilli into Ebrahim's system, because by doing so, as suggested by Arimilli the combined system will be able to efficiently divide the cache into groups of blocks called a congruence classes and thereby choose a particular memory block for eviction in order to maintain high-speed cache coherency processing in a multiprocessor computer system [e.g., Arimilli: col. 1, lines 45-57 & col. 2, lines 8-58].

As to claim 3, except the features recited in claim 2, the combined system of Ebrahim and Arimilli further discloses that the first mask value represents which of the elements of the resource are available for access for a selected component [Ebrahim: col. 6, lines 23-39; col. 14, lines 39-57].

As to claim 4, Ebrahim discloses the features as claimed by applicant, comprising:

a) a memory resource having a plurality of addressable blocks [e.g., Ebrahim: the units 108, 109, Fig. 1];

b) first and second components adapted to access the memory resource [e.g., Ebrahim: the units: 104-1 to104-n, 120-1 to 120-n, 110, 112, 132, 134-1 to 134-n, etc, Fig(s). 1 and 12 and associated texts]; and

c) an access controller having a register adapted to store a first mask value, wherein access to addressable blocks of the memory resource is controlled

based on the first mask value [e.g., Ebrahim: the System Controller (SC, 110, Fig. 5) includes SC ID register (180, Fig. 5) and SC Configure Register (190, Fig. 5) wherein, the register 180 stores the UPANUM mask filed (182, Fig. 5) and the register 190 stores the Cache Index Mask (CIM) field 194 for the system controller 110 to address blocks of memory resource based on the first mask value (e.g., the UPANUM) and associated texts].

Ebrahim does not specifically disclose the addressable blocks of the resource are selectively partitioned and access the partitioned elements thereby.

However, Arimilli et al. (hereinafter referred as Arimilli) discloses the claimed features [e.g., col. 2, lines 8-58 & the Alternate Victim Selection Logic, Fig. 3 and associated texts].

Ebrahim and Arimilli are both in the same field to improving shared cache processing via memory mask, therefore, with the teachings of Ebrahim and Arimilli in front of him/her, it would have been obvious for an ordinary skilled person in the art at the time the invention was made being motivated to combine the well-known technique as taught by Arimilli into Ebrahim's system, because by doing so, as suggested by Arimilli the combined system will be able to efficiently divide the cache into groups of blocks called a congruence classes and thereby choose a particular memory block for eviction in order to maintain high-speed cache coherency processing in a multiprocessor computer system [e.g., Arimilli: col. 1, lines 45-57 & col. 2, lines 8-58].

As to claim 5, except the features cited in claim 4, the combined system of Ebrahim and Arimilli further discloses that the memory resource is a cache memory [e.g., Ebrahim: Abstract, lines 1-5].

As to claim 6, except the features cited in claim 4, the combined system of Ebrahim and Arimilli further discloses that a processor couple to the cache memory, wherein the first component includes execution of instructions by the processor from a first thread and the second component includes execution of instructions by the processor from a second thread [e.g., Ebrahim: the unit 100, 102, Fig. 1 and associated texts; col. 6, lines 14-22; col. 17, lines 61 – col. 18, line 26; Fig(s). 5-7 and associated texts].

As to claim 7, except the features cited in claim 6, the combined system of Ebrahim and Arimilli further discloses that the first mask value represent which of the addressable blocks of the cache memory are available for eviction [e, g., Ebrahim: col. 1, lines 53-60; col. 20, lines 59 – col. 21, line 11].

As to claim 8, except the features cited in claim 7, the combined system of Ebrahim and Arimilli further discloses that the first mask value is provided for each of the components to indicate which of the addressable blocks of the cache memory are available for eviction for at least two of the components [e.g., Ebrahim: col. 1, lines 53-60; col. 20, lines 59 – col. 21, line 11; col. 31, lines 5 – 42].

As to claim 9, except the features cited in claim 7, Ebrahim further discloses an eviction array [e.g., the units: 132, 134, Fig. 1 and associated texts] and a second mask for selecting which bit of the eviction array are used for controlling which of the addressable blocks of the cache memory are available for eviction [e.g., the unit 194, Fig. 6 and associated texts].

Ebrahim did not specifically disclose that the eviction array is indicating the least recently used addressable block of the cache memory.

However, Arimilli et al. (hereinafter referred as Arimilli) discloses [col. 2, lines 39-58; the units: 44, 46, etc Fig. 2 and associated texts].

Ebrahim and Arimilli are both in the same field to process cache memory via memory mask, therefore, with the teachings of Ebrahim and Arimilli in front of him/her, it would have been obvious for an ordinary skilled person in the art at the time the invention was made being motivated to combine the well-known technique as taught by Arimilli into Ebrahim's system, because by doing so, as suggested by Arimilli the combined system will perform a must "evict" action when all of the blocks in a congruence class for a given cache are full, such that the combined system will free from memory crash. [e.g., col. 2, lines 39-58].

As to claim 10, Ebrahim discloses all limitations of claim 6, furthermore, he discloses the claimed the first mask value is an auxiliary mask value for represents which of the addressable blocks of the cache memory are available for the system to

support [e.g., the UPANUM mask filed (182, Fig. 5), Fig. 6, col. 21, lines 21 – col. 23, lines 40].

Ebrahin did not expressly discloses a eviction array wherein an auxiliary mask value for indicating and selecting the least recently used addressable block of the cache memory to evict.

However, Arimilli) discloses the claimed features [e.g., Arimilli: Fig. 3 and associated texts].

Thus, Ebrahim and Arimilli are both endeavor to optimize the process of cache memory via memory masks, therefore, with the teachings of Ebrahim and Arimilli in front of him/her, it would have been obvious for an ordinary skilled person in the art at the time the invention was made being motivated to combine the well-known technique as taught by Arimilli into Ebrahim's system, because by doing so, as suggested by Arimilli the combined system will perform real time "evict" action based on the evaluation of mask values to determine the cache hit/miss when all of the blocks in a congruence class for a given cache are full, such that the combined system will free from memory crash. [e.g., col. 2, lines 39-58; col. 7, line 41-52].

As to claims 11, 13, 18 and 20, these claims recite the same subject matter as claims 2-8 in form of method and computer program product, hence are rejected for the same reason.

(10) Response to Argument

Applicant's arguments filed on November 17, 2006 have been fully considered but they are not persuasive.

The examiner disagrees with appellant's piecemeal interpretation and arguments against the 35 U.S.C. § 103(a) rejections.

The Applicant's Invention:

A computer-implemented system and method are provided to include a resource having a plurality of elements, at least first and second components access the elements of the resource; an access controller which is coupled to a plurality of partitioned system resources, wherein accessing to the partitioned elements by the first and second components is controlled based on the first mask value.

Applicant's arguments mainly summarized as following:

The Ebrahim reference does not teach "access to the partitioned elements by said first and second components is controlled based on said first mask value" as a feature found in each of the pending independent claims.

In respond to the above arguments, the examiner directs appellants' attention to the following excerpts of Ebrahim:

"*A multiprocessor computer system has data processors and a main memory coupled to a system controller. Each data processor has a cache memory. Each cache memory has a cache controller with two ports for receiving access requests. A first port receives access requests from the associated data processor and a second port receives access requests from the system*

controller... The first mode of operation is used for all access requests by the data processor and for system controller access requests when the mode flag has a first value. The second mode of operation is used for the system controller access requests when the mode flag has a second value distinct from the first value." (Abstract)

The texts of the above excerpt clearly indicate that a first system controller component coupled to a second data processors components via two ports, wherein, the system controller and each data processor including a cache controller access the partitioned main memory elements (e.g., the memory banks of unit 108, Fig. 1) based on the settings of different values of the operational mode flags, as such, the system controller and the data processors definitely represent the claimed first and second components for controlling the access of the claimed resource elements.

In addition, the examiner directs appellants' attention to Fig 5 of Ebrahim's invention, wherein, Ebrahim clearly discloses the System Controller (e.g., SC 110, Fig. 5) includes SC ID register (e.g., the unit 180, Fig. 5, col. 21, lines 62-64) and SC Configure Register (e.g., the unit 190, Fig. 5, col. 21, line 65 – col. 22, line 4) wherein, the register 180 stores a first mask "UPANUM" which is a 5-bit mask value field that specifies the maximum number of Universal Port Architecture (UPA) ports the System Controller can support (e.g., 182, Fig. 5, col. 22, lines 8-10). The register 190 stores the Cache Index Mask (CIM) which specifies the number of Etag block entries or lines in the coherent cache, if any, of the corresponding UPA port (e.g., the unit 194, Fig. 5, col. 36-43). These mask fields were dynamically set by the system controller (e.g., the unit 110, Fig. 5) for controlling the accessing of partitioned memory resource blocks

based on the first "UPANUM" mask value (e.g., the unit 108, Fig. 1) as depicted by Ebrahim's excerptions as following:

"Referring to FIG. 1 and 2, there may be multiple address busses 114 in the system, with up to four UPA ports 104 on each UPA address bus 114. The precise number of UPA address busses is variable, and will generally be dependent on system speed requirements. Since putting more ports on an address bus 114 will slow signal transmissions over the address bus, the maximum number of ports per address bus will be determined by the signal transmission speed required for the address bus." (col. 7, line 13- col. 8, line 4)

As set forth above, the maximum port value of the system could be set up to four-port per address bus, however, this value will be determined by the data signal transmission speed.

Moreover, Ebrahim disclosed the following:

"Any request by a UPA port is herein labeled P_REQ, which stands for "port request." A port request is transmitted via the UPA port's address bus 114. If the address bus 114 is shared by more than one UPA port, the requesting port transmits its request only after it successfully arbitrates for the address bus."
"Each port request is acknowledged by the System Controller 110 via a reply message called S_REPLY. There is a dedicated point-to-point 5-bit system reply bus, S_REPLY bus 120, for each UPA port that unidirectionally sends 5-bit reply messages from the System Controller 110 to each UPA port. The System Controller 110 drives a reply code on the S_REPLY bus 120 in acknowledgment to a transaction request, and to coordinate the sourcing and sinking of data on the UPA data bus 116. More particularly, the System Controller 110 generates an S_REPLY in response to a P_REQ either when the System Controller 110 is ready to set up the data path needed to perform the requested transaction, or when the requested transaction is completed if the transaction (such as an invalidate transaction request) does not involve a data transfer. The S_REPLY message is generated by the System Controller at essentially the same time that the System Controller sends the corresponding setup signals to the interconnect module 112."

Here, as set forth above, Ebrahim clearly cited that the system controller sets up the data path needed to perform the requested data transfer transaction by using the

dedicated point-to-point 5-bit reply messages over the system bus (e.g., 120, Fig. 5), wherein, these messages have to depended on the UPANUM mask value, because if the UPANUM mask value is 0, it indicates no port is available of any address bus communication that results in no message flow between ports of any address bus, no data path connection to perform the requested transaction and no accessing of data, as such, the access to the partitioned elements by the first (e.g., the system controller) and second (e.g., the data processor) components is controlled based on the primary first mask value "UPANUM". Thereby, based on the discussion above, in contrary to appellants' arguments Ebrahim clearly teaches the claimed features.

As to the rest of arguments, appellants merely rehashed issues already addressed above.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Susan Y Chen
Examiner
Art Unit 2161

Susan Chen

Conferees

Mofiz, Apu
SPE – AU 2161

APU MOFIZ
SUPERVISORY PATENT EXAMINER

Lee, Eddie
Appeal Specialist

EDDIE C. LEE
SUPERVISORY PATENT EXAMINER